REMARKS

Reconsideration of the application is respectfully requested.

Claims 23-25 and 27-29 stand rejected under 35 U.S.C. §103(a) as being obvious in view of U.S. Patent No. 4,609,825 issued to Berger, et al. ("Berger") in view of U.S. Patent Publication 2003/0193597 issued to Fossum, et al. ("Fossum") and further in view of U.S Patent No. 7,709,259 issued to Suzuki ("Suzuki"). Applicants respectfully disagree with the rejection for the following reasons.

According to the Office Action at page 3, Berger (in Fig. 1, element 4) discloses an integrated circuit comprising a first reset shift register that has multiple outputs, where each output is coupled to control a reset of sensor elements that are in a respective one of the rows of the array (as recited in Applicants' claim 23). However, a closer review of Berger reveals that this is an incorrect analogy. Referring now to Berger, at the end of column 3 and continuing to the top of column 4,

> In the embodiment of FIG. 1, the stages of the register R_1 of the first means 4 are connected to a series of enhancement-mode MOS transistors designated by the reference TMOS-1. These transistors are connected on the one hand to one of the lines of the photosensitive zone and on the other hand to a bias voltage. **When this bias voltage is applied to the gates of the MOS-phototransistors, it permits transfer of the charges stored by these points to the columns, that is to say the reading of one line.** [Emphasis added]

Continuing now in Berger, at column 5, at approximately line 45,

> The method in accordance with the invention is applicable in the same manner when the photosensitive points consist of photodiodes. The only different in the case of photodiodes is that the voltages Vref and V_{AC} are not applied to the MOS-phototransistors but to gates which **control the transfer between the photodiodes and the columns** and which are not exposed to the radiation. [Emphasis added]

The above cited portions of Berger therefore clarify that the shift register R_1 (which is part of the means 4) is **not** coupled to control a reset of sensor elements. Rather, the means 4 carries out a **reading** of each line of photosensitive points. It therefore appears that the Examiner may have taken an unreasonably broad

interpretation of Applicants' claimed reset shift register. Indeed, where Applicants' claim recites "each output being coupled to control a reset of sensor elements of the first color ...", the Examiner appears to interpret this language as reading on the passage in Berger, at column 4, lines 24-30, which states:

> The departure of the drive pulse I_D from a stage has the effect of cutting-off the transistor TMOS-1 which is associated with this stage. At this instant, the corresponding transistor TMOS-TAC applies the voltage V_{AC} to the line which is addressed by said stage, thus **bringing to an end the reading of charges of said line and marking the start of its integration period**. [Emphasis added]

The above described reading mechanism of Berger is different than the reset of a sensor element by a reset shift register, as recited in Applicants' claim 23.

Moreover, the Examiner appears to have ignored a further limitation in Applicants' claim 23, namely that the control logic is coupled to feed each of the first and second shift registers with a **pair** of reset bits. In addition, this control logic is coupled to feed the wordline shift register (which has multiple outputs coupled to control the readout of the sensor elements) with a read bit. This additional limitation is not taught or suggested in Berger. However, the Office Action looks to Fossum which discloses the resetting of a floating diffusion output node of a single cell. However, neither Berger nor Fossum teach or suggest the above recited combination of the control logic coupled to feed each of the first and second shift registers with a pair of reset bits, and the wordline shift register with a read bit, and to operate these registers so that the reset bits and the read bit shift through their respective registers while an image frame is being captured with one of the reset bits of the pair always being one or more rows ahead of the read bit to mark the start of integration, and the other one of the pair to generate a correlated double sampling pixel reset value after each pixel integrated intensity value.

Indeed, although in Fossum the use of correlated double sampling is disclosed, this does not teach or suggest modifying the means 4 of Berger into a reset shift register as recited in Applicants' claim 23, and feeding the shift register with a pair of reset bits and providing a wordline shift register that is fed a read bit, where the pair of reset bits

and the read bit behave as recited in Applicants' claim 23. Indeed, there is no mention in Fossum of a "reset bit" but rather merely of a CMOS active pixel circuit with its operation during correlated double sampling.

As to the contention in the Office Action at page 4, that Fossum discloses sampling a reset voltage **at the end of integration**, Applicants also respectfully disagree. A review of paragraphs 28, 29, and 33 of Fossum (cited by the Examiner) does not reveal any such teaching. In paragraph 28, the floating diffusion output node 104 is first reset by pulsing a reset transistor. The resultant voltage in FD 104 is read out onto a column bus 112. The voltage on the column bus 112 is sampled onto a holding capacitor 114. This initial charge is used as the baseline. The signal charge is then transferred to FD 104 (paragraph 29). Accordingly, if anything, Fossum appears to suggest the opposite, namely that the reset voltage be produced and sampled **before**, not after, the end of integration.

In view of the foregoing, Applicants submit that a reasonable basis for finding claim 23 obvious has not been set forth in the Office Action. Moreover, the Office Action continues at page 4, to incorrectly combine Berger and Fossum with a further reference, Suzuki, which does disclose a color image sensor wherein the integration time for each color is adjustable. Applicants again respectfully submit that claim 23 is not so broad as apparently interpreted by the Examiner. The Examiner here appears to have ignored how one of ordinary skill in the art would modify the Berger or Fossum sensors into one that detects color, **using the particular reset and wordline shift register logic recited in claim 23**. The use of separate registers for each color in Suzuki does not teach or suggest the more specific arrangement of Applicants' claim 23 where reset bits and read bits are shifted through their respective registers to control the reset and readout of sensor elements in a manner that allows the reset bits to be programmed to set the integration time independently for multiple colors. In Suzuki, the use of the shift registers is only to control the readout of the photodiodes and does not appear to teach or suggest the use of the shift registers to control the integration time by the combination of the resetting of the sensors (using reset bits) and read bits.

For the above reasons, Applicants respectfully submit that the rejection of the pending claims in view of Berger, Fossum, and Suzuki is improper.

Respectfully submitted,

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Margaux Rodriguez January 7, 2004+